Analog Power AM4890N

Dual N-Channel 150-V (D-S) MOSFET

Key Features:

- Low r_{DS(on)} trench technology
- · Low thermal impedance
- · Fast switching speed

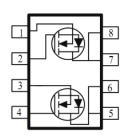
Typical Applications:

- PoE Power Sourcing Equipment
- PoE Powered Devices
- Telecom DC/DC converters
- · White LED boost converters

PRODUCT SUMMARY				
V _{DS} (V)	$r_{DS(on)}(\Omega)$	I⊳(A)		
150	$0.7 @ V_{GS} = 10V$	1.4		
130	$1.2 @ V_{GS} = 5.5V$	1.1		







ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}$ C UNLESS OTHERWISE NOTED)					
Parameter			Limit	Units	
Drain-Source Voltage	V_{DS}	150	V		
Gate-Source Voltage	V_{GS}	±20	V		
Continuous Drain Current ^a $ T_A=25^{\circ} $ $ T_A=70^{\circ} $			1.4		
		l _D	1.1	Α	
Pulsed Drain Current ^b	I _{DM}	10			
Continuous Source Current (Diode Conduction) a	I _S	2.6	Α		
Dower Dissination a	T _A =25°C		2.1	W	
Power Dissipation ^a	T _A =70°C	' D	1.3	VV	
Operating Junction and Storage Temperature Range			-55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Maximum	Units		
Maximum Junction-to-Ambient ^a	t <= 10 sec	$R_{\theta JA}$	62.5	°C/W	
Maximum Junction-to-Ambient	Steady State	IN _θ JΑ	110	C/VV	

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Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

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Parameter	Symbol	Test Conditions		Тур	Max	Unit
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \text{ uA}$	1			V
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = 20 \text{ V}$			±100	nA
Zero Gate Voltage Drain Current	Yoro Cata Voltago Drain Current				1	uA
Zero Gate Voltage Brain Gurrent	I _{DSS}	$V_{DS} = 120 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			10	u/\
On-State Drain Current	I _{D(on)}	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	0.5			Α
Drain-Source On-Resistance	r _{no()}	$V_{GS} = 10 \text{ V}, I_D = 1.2 \text{ A}$			0.7	Ω
Dialii-Source Off-Nesistance	r _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 1.1 \text{ A}$			1.2	12
Forward Transconductance	g _{fs}	$V_{DS} = 15 \text{ V}, I_{D} = 1.2 \text{ A}$		11		S
Diode Forward Voltage	V_{SD}	$I_S = 1.3 \text{ A}, V_{GS} = 0 \text{ V}$		0.8		V
		Dynamic				
Total Gate Charge	Q_g			3.7		
Gate-Source Charge	Q_gs	$V_{DS} = 75 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 1.2 \text{ A}$		1.3		nC
Gate-Drain Charge	Q_{gd}			1.8		
Turn-On Delay Time	t _{d(on)}			5		
Rise Time	t _r	$V_{DD} = 75 \text{ V}, R_L = 62.5 \Omega, I_D = 1.2 \text{ A},$		10		nc
Turn-Off Delay Time	t _{d(off)}	$V_{GEN} = 10 \text{ V}, R_{GEN} = 6 \Omega$		16		ns
Fall-Time	t _f			8		
Input Capacitance	C_{iss}			347		
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		37		pF
Reverse Transfer Capacitance	C_{rss}			20		

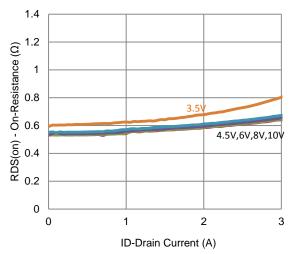
Notes

- a. Pulse test: PW <= 300us duty cycle <= 2%.
- b. Guaranteed by design, not subject to production testing.

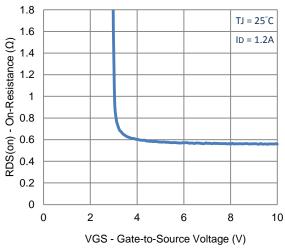
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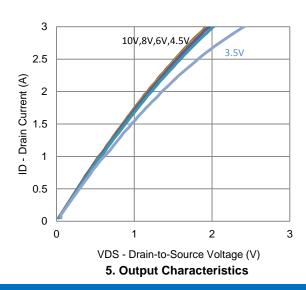
Typical Electrical Characteristics

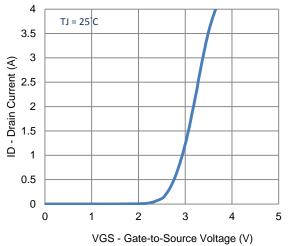


1. On-Resistance vs. Drain Current

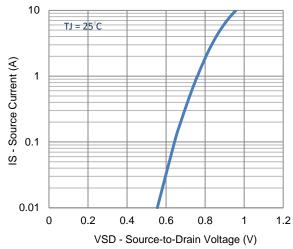


3. On-Resistance vs. Gate-to-Source Voltage

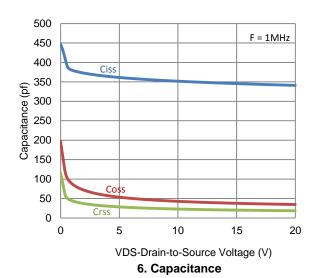




2. Transfer Characteristics

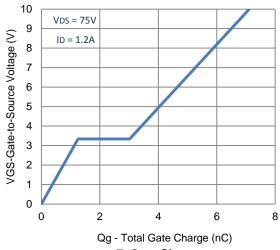


4. Drain-to-Source Forward Voltage

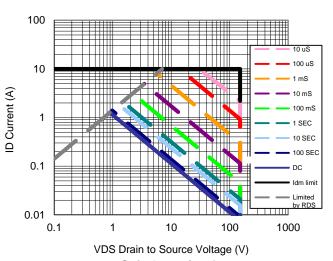


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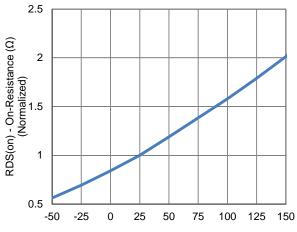
Typical Electrical Characteristics





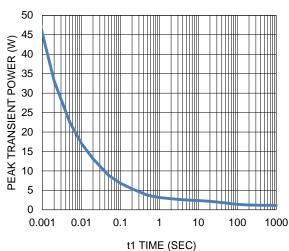


9. Safe Operating Area

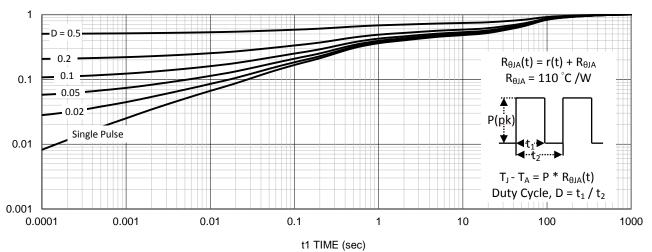


TJ - Junction Temperature (°C)

8. Normalized On-Resistance Vs **Junction Temperature**



10. Single Pulse Maximum Power Dissipation

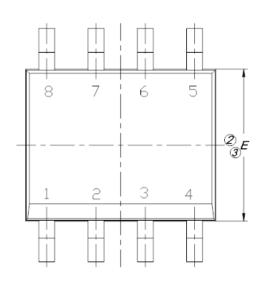


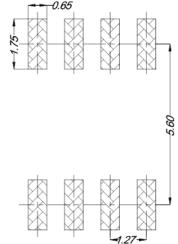
11. Normalized Thermal Transient Junction to Ambient

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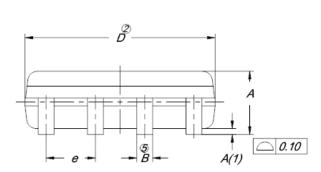
Package Information

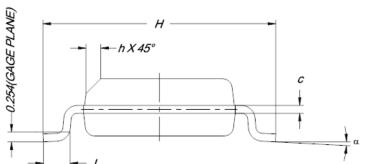
Land Pattern (Only for Reference)





5114	MILLIMETERS				
DIM.	MIN.	NOM.	MAX.		
Α	1.35	1.55	1.75		
A(1)	0.10	0.18	0.25		
В	0.38	0.45	0.51		
С	0.19	0.22	0.25		
D	4.80	4.90	5.00		
E	3.80	3.90	4.00		
е	1.27 BSC				
Н	5.80	6.00	6.20		
L	0.50	0.72	0.93		
α	0°	4°	8°		
h	0.25	0.38	0.50		





Note:

- All Dimension Are In mm.
- Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
- 3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
- 4. The Package Top May Be Smaller Than The Package Bottom.
- 5. Dimension B" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.08 mm Total In Excess Of "B" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.